REMARKS

Claims 1-40 are pending in the present application. In the Office Action dated March 22, 2006, the Examiner took the following action: (1) rejected claims 1-5, 37 and 40 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,229,727 to Doyle ("Doyle"); (2) rejected claims 6-19, 21, 24-26, 31-33 and 36 under 35 U.S.C. § 103(a) as being unpatentable over Doyle and further in view of U.S. Patent No. 6,667,895 to Jang et al. ("Jang"); (3) rejected claims 20 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Doyle in view of Jang as applied to claims 13, 19 and 26 and further in view of U.S. Patent No. 5,465,229 to Bechtolsheim et al. ("Bechtolsheim"); and (4) rejected claims 22-23, 28-30, 34-35 and 38-39 under 35 U.S.C. § 103(a) as being unpatentable over Doyle in view of Jang as applied to claims 19, 26 and 37 and further in view of U.S. Patent No. 6,272,609 to Jeddeloh ("Jeddeloh").

Discussion of technological examples

Disclosed embodiments of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

A disclosed example of the invention is a method for applying appropriate address and control signals to interconnected memory devices using a memory hub to couple different signals to various bus lines depending on which particular memory device is being accessed. (See Specification, ¶27). The memory devices may be mounted on different surfaces of a substrate and have interconnected terminals (See Specification, ¶ 25). At least in part because the memory hub applies the appropriate signals to the bus depending on which memory device is being accessed, the interconnected memory devices themselves need not have any special, or mirrored, configuration or internal routing of the received signal to the appropriate terminal. (See Specification, ¶ 27).

The Examiner cited U.S. Patent Number 6,229,727 to Doyle ("Doyle") under 35 U.S.C. § 102(b). Doyle discloses an apparatus and method for supporting multiple configurations or sizes of memory in a single socket architecture. (See Abstract). Doyle's disclosure addresses the problem created by placing memories with differing addressing schemes into a single provided DIMM socket (see col. 1, lines 52-66). Doyle discloses a multiplexer configured to output the appropriate configuration of signals to a single DIMM socket based on the particular type of memory device installed in the socket (see col. 6, lines 31-43). As indicated in Doyle's Figure 1, several DIMM sockets may be provided in parallel (see Fig. 1, DIMM socket 20 and DIMM socket 22). Doyle fails to disclose or suggest interconnecting memory devices to each other in a manner that causes identical memory devices to function differently responsive to address and control signals applied to the interconnected terminals. Doyle further fails to disclose or suggest applying address and control signals to the interconnected terminals depending on which of the identical memory devices is being accessed. Still further, Doyle fails to disclose or suggest connecting devices in a mirror configuration. Doyle's DIMM sockets simply receive information from the same bus (see Fig. 2, bus 18).

The Examiner cited U.S. Patent Number 6,667,895 to Jang ("Jang") under 35 U.S.C. § 103(a). Jang discloses switching circuitry, internal to an integrated circuit, that allow a user to reconfigure the effective pin assignments for the integrated circuit pads. (See col. 6, lines 7-16). Utilizing Jang's internal switching circuitry allows two identically fabricated integrated circuits to be configured effectively as either a normal pin configuration chip or a "mirrored pin configuration" chip (see Jang, Figs. 1 and 2, col. 6, lines 18-29). When two chips are connected together in a mirrored configuration, the internal switching circuitry routes the identically arranged memory signals to the appropriate pad on the chip, depending on if the chip is configured as a "normal" or "mirrored" chip. (See col. 7, lines 14-24). Jang does not disclose rearranging the configuration of the applied signals themselves.

Patentabilty over Doyle

Turning, now to the claims, independent claims 1 and 37 have been amended to specify that memory devices are disposed on two surfaces of a substrate. For this and other

reasons, independent claims 1 and 37 are novel over Doyle which, as explained above, fails to disclose interconnecting memory devices on two surfaces of a substrate.

Claims depending from independent claims 1 and 37 are also allowable and distinguished over Doyle because of their dependency on patentable independent claims and because of the additional limitations added by those claims. Accordingly, Applicant respectfully submits that the 35 U.S.C. § 102(b) rejection of claims 1-5, 37, and 40 has been overcome and should be withdrawn.

Patentability over Doyle in view of Jang

As an initial matter, Applicant respectfully submits that there is no motivation to combine the teaching of Jang with that of Doyle. Doyle's system applies the appropriately arranged signals to a DIMM socket depending on the pin layout of the memory device in the DIMM socket. Jang's system provides memory devices that receive signals and pass the received signals through internal switching circuits such that the signals are connected to the appropriate internal pads of the mirrored integrated circuit. Placing Jang's integrated circuits into the DIMM sockets of Doyle would not require rearranging of the signals applied to the memory devices, because Jang's memory devices contain their own internal routing circuits. Neither reference discloses or suggests interconnecting memory devices to each other in a manner that causes the identical memory devices to function differently responsive to address and control signals applied to the interconnected terminals, and then applying address and control signals to the interconnected terminals differently depending on which device is being accessed.

Independent claims 6, 12, 19, 26, and 33 have been amended to specify that interconnected memory devices each operate differently responsive to a received signal at their interconnected terminals. As discussed above, Jang, in contrast, provides interconnected chips that operate identically due to Jang's disclosed internal signal routing system.

Claims depending from independent claims 6, 12, 19, 26, and 23 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. Applicant therefore respectfully requests the 35 U.S.C. § 103(a) rejection over Doyle in view of Jang be withdrawn.

As a final matter, Applicant notes a Supplemental Information Disclosure Statement filed April 14, 2006. Acknowledgement of consideration of the information therein is respectfully requested. All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,
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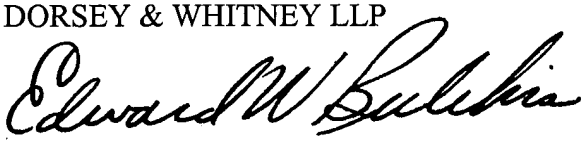

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